VT

COFC

PATENT

I hereby certify that on the date specified below, this correspondence is being deposited with the United States Postal Service as first-class mail in an envelope addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

April 3, 2008
Date

Jennifer A. Steele
Jennifer A. Steele

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants	: Christopher K. Morzano and Wen Li	Attorney Docket No.:	501284.01
Serial No.	: 10/617,246	Patent No.	: US 6,922,367 B2
Filed	: July 9, 2003	Issue Date	: July 26, 2005
Title	: DATA STROBE SYNCHRONIZATION CIRCUIT AND METHOD FOR DOUBLE DATA RATE, MULTI-BIT WRITES		

REQUEST FOR CORRECTED CERTIFICATE OF CORRECTION

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Attached is the original official Certificate of Correction received from the PTO in the above-identified application, for which issuance of a corrected Certificate of Correction is respectfully requested.

There is an error in Column 3, Lines 65-67, wherein a comma appears at the end of the first sentence, following the word, "time". There should be a period instead of a comma.

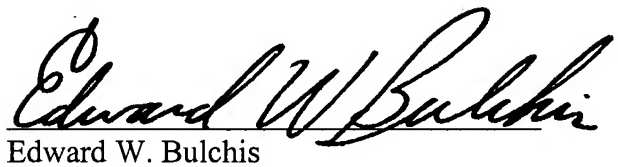
Also, the Certificate of Correction incorrectly lists "Column 8, lines 14-15 as the portion being corrected. This should read, "Column 8, lines 13-14." The wording that is associated with these lines is otherwise correct.

Column, Line	Reads	Should Read
Column 3, Lines 65-67	"Returning to FIG. **1**, since the ENA and ENB signals that enable the logic circuits **46**, **48** are generated by a flip-flop **60**, they are enabled at the same time,"	-- Returning to FIG. **1**, since the ENA and ENB signals that enable the logic circuits **46**, **48** are generated by a flip-flop **60**, they are enabled at the same time.--
Column 8, Lines 14-15 [Should Read: Column 8, Lines 13-14]	[The wording associated with these lines is otherwise correct.]	

The corrections to be made have been marked in red on the original of the enclosed Certificate of Correction.

Respectfully submitted,

DORSEY & WHITNEY LLP



Edward W. Bulchis
Registration No. 26,847

EWB:
Enclosures:
Postcard
Original Certificate of Correction (with changes marked in red)

1420 Fifth Avenue, Suite 3400
Seattle, WA 98101
Tel: (206) 903-8800
Fax: (206) 903-8820

h:\ip\clients\micron technology\1200\501284.01\501284.01 req corrected cert of corr.doc

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 6,922,367 B2
APPLICATION NO. : 10/617246
DATED : July 26, 2005
INVENTOR(S) : Christopher K. Morzano and Wen Li

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column, Line	Reads	Should Read
Item (57), Line 3	"respective enable signal"	--a respective enable signal--
Column 1, Line 51	"conventional DDR memory device,"	--conventional DDR memory devices,--
Column 2, Line 31	"diagram a data strobe"	--diagram of a data strobe--
Column 3, Lines 31 and 32	"complimentary"	--complementary--
Column 3, Line 57	"compliment"	--complement--
Column 3, Lines 65-67	"Returning to FIG. **1**, since the logic circuits **46**, **48**, the ENA and ENB signals that enable the logic circuits **46**, **48** are generated by a flip-flop."	--Returning to FIG. **1**, since the ENA and ENB signals that enable the logic circuits **46**, **48** are generated by a flip-flop **60**, they are enabled at the same time.--
Column 5, Line 62	"through the nor gate"	--through the NOR gate--
Column 6, Line 9	"and RAMBUS DRAMs (RDRAMS"),"	--and RAMBUS DRAMs ("RDRAMS"),--
Colum 6, Line 18	"memory arrays **120**, **12**"	--memory arrays **120**, **122**--
Column 7, Line *5*	"which the"	--with the--
Column 8, Line 9	"applied to control input"	--applied to a control input--
Column 8, Line 13 ~~13~~ 14	"being compliments"	--being complements--
Column 8, Lines ~~14-15~~	"logic circuit in enabled"	--logic circuit is enabled--
Column 8, Line 30	"coupled to reset"	--coupled to the reset--
Column 9, Line 23	"applied to an control input"	--applied to a control input--
Column 9, Line 27	"compliments"	--complements--
Column 9, Lines 28-29	"logic circuit in enabled"	--logic circuit is enabled--
Column 9, Lines 43-44	"coupled to reset input"	--coupled to the reset input--
Column 10, Line 33	"coupled the external data terminal"	--coupled to the external data terminal--
Column 10, Line 40	"applied to an control input"	--applied to a control input--
Column 10, Line 44	"being compliments"	--being complements--
Column 10, Lines 45-46	"second logic circuit in enable"	--second logic circuit is enabled--

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 6,922,367 B2
APPLICATION NO. : 10/617246
DATED : July 26, 2005
INVENTOR(S) : Christopher K. Morzano and Wen Li

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column, Line	Reads	Should Read
Column 10, Line 61	"coupled to reset"	--coupled to the reset--
Column 12, Line 12	"applied to an control input"	--applied to a control input--
Column 12, Line 16	"compliments"	--complements--
Column 12, Lines 17-18	"logic circuit in enabled"	--logic circuit is enabled--
Column 13, Lines 28-29	"being operable to generate make the first enable signal"	--being operable to make the first enable signal--
Column 13, Line 43	"applied to an control input"	--applied to a control input--
Column 13, Line 47	"compliments"	--complements--
Column 13, Line 48-49	"logic circuit in enabled"	--logic circuit is enabled--
Column 13, Line 63	"circuit farther"	--circuit further--
Column 15, Line 28	"applied to an control input"	--applied to a control input--
Column 15, Line 32	"compliments"	--complements--
Column 15, Lines 33-34	"logic circuit in enabled"	--logic circuit is enabled--
Column 16, Lines 5 and 17	"the method comprises:"	--the method comprising:--

Signed and Sealed this

Twenty-fifth Day of December, 2007

JON W. DUDAS
Director of the United States Patent and Trademark Office